INVERSE-MODIFIED DISCRETE COSINE TRANSFORM AND OVERLAP-ADD METHOD AND HARDWARE STRUCTURE FOR MPEG LAYER3 AUDIO SIGNAL DECODING

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention generally relates to a method and hardware structure for audio signal decoding, and more particularly, to an inverse-modified discrete cosine transform and overlap-add method and hardware structure for MPEG Layer3 audio signal decoding.

Description of Related Art

[0002] Digital audio signal processing is widely used. This is because the digital audio signal immunity to noise is higher than the analog signal. However, since it is quite often demanded to process a large amount of data within a very short time and still needs to maintain the effect of high audio quality, a lot of the audio signal compression standards have been developed. The motion picture experts group (abbreviated as MPEG) standard is widely accepted due to its high compression rate and low distortion. MPEG, using the different sensitivity of the human ear to different frequency bands, assigns fewer bits to the audio to which the human ear is not so sensitive, to achieve the objective of compression.

[0003] Furthermore, in order to accommodate different levels of audio quality with the compression method, MPEG is further divided into Layer1, Layer2 and Layer3. Generally speaking, the higher the level of the layer, the more complicated the compression method, the distortion of the corresponding recovered audio signal is much

less, and the effect is better.

[0004] The encoding process of MPEG can be divided into the encoder and the decoder portions. In the encoder portion, the audio data is processed and converted into 32 data sub-bands by using the analysis sub-band filter bank. Then, the data belonging to different bands can be assigned to different bits according to the psycho-acoustical model that simulates the artificial ear acoustic effect. Afterwards, the objective of the compression can be achieved via quantization. Finally, the data is sent out in a specific data format framing.

[0005] The decoder portion looks like the reverse operation of the encoder. The data is unpacked first, and after the inverse quantization process, the 32 data sub-bands are integrated into the original audio data by using the synthesis sub-band filter bank.

[0006] As to the MPEG-II audio encoding standard, multi-channel audio encoding is further provided, while all the other aspects are basically the same as the MPEG I. Multi-channel audio can be divided into the Left (L) and Right (R) channel audio transmitted via the basic transmission channels T0, T1, and the Central (C), Left Surround (LS) and Right Surround (RS) channel audio transmitted via the extended transmission channels T2, T3, T4. The multichannel decoder is needed for the MPEG-II audio decoding to reconstruct the multichannel audio signal.

[0007] The MPEG LAYER3 compression standard, using the MPEG Layer3 (MP3) compression algorithm, is widely used in the application of digital broadcast and multimedia. As to the digital audio signal compression, MP3 is the most complicated algorithm, providing the highest compression rate within MPEG. MP3 utilizes the inverse-modified discrete cosine transform (hereinafter abbreviated as IMDCT) and the sub-band coding techniques, whereby MP3 can achieve such high compression rate.

[0008] The hardware structure of MPEG Layer1 and Layer2 decoders has already been physically implemented by many researchers. However, there is no appropriate hardware structure to implement MP3. Most of the hardware structure design nowadays is implemented using the general digital signal processor (abbreviated as DSP). This design

5 utilizes program control to achieve the objective. However, a large amount of memory is needed for this design to store the program code, and thus the hardware burden and area is increased, so that the performance of the entire system cannot achieve the optimum.

SUMMARY OF THE INVENTION

10 [0009] The present invention provides an inverse-modified discrete cosine transform and overlap-add method and hardware structure for MPEG Layer3 audio signal decoding. The present invention implements the entire hardware structure via the high speed algorithm of the inverse-modified discrete cosine transform and overlap-add, so that the entire system is able to fulfill the low cost and high performance requirements.

15 [0010] In order to at least achieve the objective mentioned above and other objectives, the present invention provides an inverse-modified discrete cosine transform and overlap-add method for MPEG Layer3 audio signal decoding. At first, the 32 sub-band samples of the compressed audio signal are applied with the operation of the inverse-modified discrete cosine transform and overlap-add according to equation (1),

20 inverse-modified discrete cosine transform:

$$x(i) = \sum_{k=0}^{\frac{n}{2}-1} X(k)*\cos(i,k) \qquad 0 \le i \le \frac{n}{4}-1 \text{ and } \frac{n}{2} \le i \le \frac{3n}{4}-1$$

overlap-add:

$$Z(i) = x(i) * win(i,p)$$

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$$Z(\frac{n}{2}-1-i) = -x(i) * win(\frac{n}{2}-1-i, p) \quad 0 \leq i \leq \frac{n}{4}-1$$

$$Z(i) = x(i) * win(i, p)$$

$$Z(n-1-i) = x(i) * win(n-1-i, p) \quad \frac{n}{2} \leq i \leq \frac{3n}{4}-1 ,$$

5   where X(k) is the sub-band sample and Z(i) is the sub-band sample after process. When

window type is 0, 1, 3, n equals 36; whereas when window type is 2, n equals 12. Then,

the dynamic window inverse-modified discrete cosine transform module is provided.

The operation of the inverse-modified discrete cosine transform is processed by the

multiplier-adder of the dynamic window inverse-modified discrete cosine transform

10   module. The result after the operation of the inverse-modified discrete cosine transform

is stored in the register stack of the dynamic window inverse-modified discrete cosine

transform module. Afterwards, the operation of the overlap-add is processed by the

multiplier-adder, and the result after the operation of the overlap-add is stored in the

buffer memory of the dynamic window inverse-modified discrete cosine transform

15   module.

[0011]   The present invention further provides an inverse-modified discrete cosine

transform and overlap-add hardware structure for MPEG Layer3 audio signal decoding.

The hardware structure comprises the dynamic window inverse-modified discrete cosine

transform module and the dynamic window inverse-modified discrete cosine transform

20   buffer memory. The dynamic window inverse-modified discrete cosine transform

module comprises the multiplier-adder and the register stack. The multiplier-adder is

used to calculate the inverse-modified discrete cosine transform and overlap-add, the

register stack is coupled to the multiplier-adder and is used to store the operation result of

the inverse-modified discrete cosine transform. The dynamic window inverse-modified discrete cosine transform buffer memory is coupled to the dynamic window inverse-modified discrete cosine transform module and is used to store the operation result of the overlap-add.

5   [0012] In summary, the present invention implements the entire hardware structure by using the fast algorithm of the dynamic window inverse-modified discrete cosine transform and overlap-add, and makes the entire system fulfill the lost cost and high performance requirements.

10   BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention. In the drawings,

15   [0014] FIG. 1 schematically shows the decoding flow chart of the MP3 of the inverse-modified discrete cosine transform and overlap-add method and hardware structure for MPEG Layer3 audio signal decoding according to the present invention;

[0015] FIG. 2 schematically shows the flow chart of the inverse-modified discrete cosine transform and overlap-add method for MPEG Layer3 audio signal decoding of a

20   preferred embodiment according to the present invention;

[0016] FIG. 3 schematically shows the hardware structure diagram of the inverse-modified discrete cosine transform and overlap-add hardware structure for MPEG Layer3 audio signal decoding of a preferred embodiment according to the present invention;

[0017] FIG. 4 schematically shows the layout diagram of the DWIMDCT buffer memory

of FIG. 3; and

[0018]   FIG. 5 schematically shows the sketch map of the sequence of writing of the memory bank in the DWIMDCT buffer memory and the sequence of reading of the synthesis filter bank.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019]   The present invention is suitable for the MPEG Layer3, but no matter whether MPEG-I or MPEG-II, the audio signal can all be decoded.   As to digital audio signal compression, MP3 is the most complicated algorithm, and also provides highest

10   compression rate.   Therefore, the preferred embodiment provided by the present invention is aimed at the entire MP3 compression algorithm, so as to reduce the quantity of the data and operation.   Thus, the fast algorithm is provided accordingly.   Then, the entire hardware structure is implemented by using the fast algorithm, so that the entire system fulfills the low cost and high performance requirements.

15   [0020]   FIG. 1 schematically shows the decoding flow chart of the MP3 of the inverse-modified discrete cosine transform and overlap-add method and hardware structure for MPEG Layer3 audio signal decoding according to the present invention. The whole flow can be divided into the pre-process portion 10 and the post-process portion 12.   The pre-process portion 10, first obtains the bit stream and finds out the head 10 (step s102).   It

20   then decodes the remark information (step s104), decodes the proportion factor (step s106), and decodes the Huffman data (step s108).   Afterwards, it re-arranges the frequency spectrum line (step s110), and incorporates the stereo process (if it is used) (step s112).   Finally, it eliminates the return distortion (step s114).   The pre-process portion 10 is mostly used for the process of the bit stream.   In general, the operation

quantity for this portion is not so large. However, the process is very fussy, and thus this portion generally can be implemented by using the finite state machine and the embedded micro-controller, so that the entire system design can be effectively simplified. There has been a lot of research aimed at this portion in recent years.

5   [0021] The post-process portion 12 mostly comprises the synthesis process of the inverse-modified discrete cosine transform (abbreviated as IMDCT) and the overlap-add of the present invention (these two processes cooperate and are called the dynamic window inverse-modified discrete cosine transform (abbreviated as DWIMDCT)) (step s116) and also the process of the synthesis filter bank (step s118). After the process of the

10   synthesis filter bank, the pulse code modulation sample is output (step s120). In general, the quantity of the operation of the post-process 12 is larger than the pre-process 10, and takes about 80% of the whole process. Because of this, the post-process 12 needs to be implemented by an appropriate hardware structure, so that the entire system can fulfill the low cost and high performance requirements.

15   [0022] In order to have the entire system fulfill the low cost and high performance requirements, the present invention provides a flow chart of a preferred embodiment using the inverse-modified discrete cosine transform and overlap-add method for MPEG Layer3 audio signal decoding (that is the IMDCT fast algorithm), as shown in FIG. 2. The 32 sub-band samples of the compressed audio signal are applied with the operation of

20   the inverse-modified discrete cosine transform and overlap-add by the IMDCT fast algorithm according to equation (1),

inverse-modified discrete cosine transform:

$$x(i) = \sum_{k=0}^{\frac{n}{2}-1} X(k) * \cos(i,k) \qquad 0 \le i \le \frac{n}{4} - 1 \text{ and } \frac{n}{2} \le i \le \frac{3n}{4} - 1$$

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overlap-add:

$$Z(i) = x(i) * win(i, p)$$

$$Z(\frac{n}{2} - 1 - i) = -x(i) * win(\frac{n}{2} - 1 - i, p) \quad 0 \le i \le \frac{n}{4} - 1$$

$$Z(i) = x(i) * win(i, p)$$

5 $$Z(n - 1 - i) = x(i) * win(n - 1 - i, p) \quad \frac{n}{2} \le i \le \frac{3n}{4} - 1 \quad ,$$

where X(k) is the sub-band sample, Z(i) is the sub-band sample after process, when

window type is 0, 1, 3, n equals 36; whereas when window type is 2, n equals 12. The

equation (1) above indicates that the quantity of the operation can be reduced from n to

n/2. That is, the quantity of the operation of the inverse-modified discrete cosine

10 transform in the DWIMDCT can be reduced by half. Table 1 lists the comparison of the

quantity of the operation of the original and the present invention. As shown in Table 1,

when the window type is 0, 1, 3, the ratio of the present invention to the original is 0.48

MOPS (million operation per second). When the window type is 2, the ratio of the

present invention to the original is 0.42 MOPS. Therefore, the quantity of the operation

15 of the inverse-modified discrete cosine transform can be significantly reduced.

Table 1

Function	Window Type	Original	Present Invention	Ratio (MOPS)
IMDCT	Type 0,1,3	2.1	1	0.48
	Type 2	1	0.42	0.42

[0023]   Afterwards, the entire hardware structure is implemented by using the fast algorithm. FIG. 3 schematically shows the hardware structure diagram of the inverse-modified discrete cosine transform and overlap-add hardware structure for MPEG Layer3 audio signal decoding of a preferred embodiment according to the present invention. The hardware structure comprises the DWIMDCT module 30 and the DWIMDCT buffer memory 32. Wherein, the DWIMDCT module 30 mostly comprises the multiplier-adder (MAC0) 302 and the register stack 304. The operation method of the hardware structure is described hereafter.

[00024]   At first, the multiplier-adder 302 is utilized by the inverse-modified discrete cosine transform for calculation, and the final result is subsequently stored in the register stack 304. The register stack 304 comprises 18 registers. After the operation of the inverse-modified discrete cosine transform, the overlap-add of the dynamic window is the follow-on operation. The operation of the overlap-add of the dynamic window is also accomplished by using the multiplier-adder 302, and the final result is stored in the DWIMDCT buffer memory 32. FIG. 4 schematically shows the layout diagram of the DWIMDCT buffer memory 32. As is shown in the diagram, the DWIMDCT buffer memory 32 comprises 3 memory banks (memory bank 0, memory bank 1 and memory bank 2), each memory bank can be further divided into 32 sub-band blocks, and each sub-band block is able to store 18 sample data. Furthermore, the hardware structure and the synthesis filter bank of the present invention are able to form a two-stage high performance pipeline process. The sequence of the DWIMDCT writing of the sample data contained in each memory bank of the DWIMDCT buffer memory 32 and the sequence of the reading of the synthesis filter bank are shown in FIG. 5.

[0025]   The hardware structure of the inverse-modified discrete cosine transform and

overlap-add for MPEG Layer3 audio signal decoding according to the present invention is easily compatible with the hardware of other modules, and is suitable for the design of the very large scale integration (VLSI). If the synthesis filter bank module can be integrated, the hardware utilization will be significantly enhanced, as will the operation

5   performance of the entire decoder. Therefore, the MPEG Layer3 can be implemented by the ASIC, so that the entire system can fulfill the low cost and high performance requirements.

[0026] In summary, the present invention bears the following advantages:

1. The present invention provides a low cost fast algorithm of the inverse-

10   modified discrete cosine transform and overlap-add.

2. The present invention provides a hardware structure that is suitable for the inverse-modified discrete cosine transform and overlap-add in the MPEG Layer3 decoder.

3. The hardware structure of the present invention makes the MPEG Layer3 able

15   to be implemented by the ASIC, so that the entire system fulfills the low cost and high performance requirements.

[0027] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the

20   spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.